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ASIC Implementation of a MIMO-OFDM Transceiver for 192 Mbps WLANs

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Abstract:

Next generation wireless local area networks (WLANs) such as the IEEE 802.11n standard are expected to rely on multiple antennas at both transmitter and receiver to increase throughput and link reliability. However, these improvements come at a significant increase in signal processing and hence hardware complexity compared to existing single-antenna systems. This paper presents, to the best of the authors' knowledge, the first 4×4 MIMO-OFDM WLAN physical layer ASIC based on the OFDM specifications of the IEEE 802.11a standard. The ASIC achieves an uncoded throughput of 192 Mbps in a 20 MHz channel resulting in a spectral efficiency of 9.6 bits/s/Hz. We describe the hardware architectural differences to single-antenna OFDM systems as well as the extensions made necessary by the use of multiple antennas. Our implementation provides reference for the silicon complexity of MIMO-OFDM systems.

1. Introduction

Multiple-input multiple-output (MIMO) systems [1, 2] employ multiple antennas at both transmitter and receiver to significantly improve link reliability and throughput of wireless communication systems. These gains come at no additional transmit power or bandwidth expenditure.

MIMO is considered the key enabling technology for future wireless local area networks (WLANs) and wireless local loop (WLL) systems targeting peak data rates of up to 1 Gbps [3].

IEEE 802.11a [4] is an established WLAN standard that provides data rates of up to 54 Mbps using single-input single-output (SISO) antenna technology and employing orthogonal frequency division multiplexing (OFDM) modulation. The use of OFDM drastically simplifies equalization and consequently receiver design. MIMO technology in combination with OFDM is therefore expected to constitute the basis for the upcoming IEEE 802.11n standard, which extends the IEEE 802.11a standard to higher data rates by using up to four antennas at both transmitter and receiver.

While ASICs for the IEEE 802.11a standard have been presented (e.g. [5]), little is known about suitable VLSI architectures for MIMO-OFDM systems and the corresponding silicon complexity. To the best of our knowledge no ASIC implementation of a MIMO-OFDM WLAN transceiver with up to four transmit and receive antennas has been reported in the literature to date.

Contributions: In this paper an ASIC implementation of the baseband signal processing unit of a 4×4 MIMO-OFDM transceiver is described. The basic system architecture is based on the SISO IEEE 802.11a Physical Medium Dependent (PMD) layer and is therefore most relevant to the upcoming MIMO-based IEEE 802.11n standard. Our ASIC achieves uncoded data rates of up to 192 Mbps in a 20 MHz channel corresponding to a maximum spectral efficiency of 9.6 bits/s/Hz. The VLSI implementation reported in this paper quantifies the true silicon complexity of a MIMO-OFDM WLAN transceiver and provides reference for the increase in silicon complexity due to the use of MIMO technology.

Outline of the paper: In Section 2, we start with a brief description of the basic MIMO-OFDM system setup considered in this paper. The high-level VLSI architecture and the implementation of the MIMO-OFDM transceiver including MIMO detection are described in Section 3. In Section 4, the hardware complexity of the resulting silicon implementation is assessed and compared to the corresponding complexity of a SISO-based OFDM system. Conclusions are drawn in Section 5.

2. MIMO-OFDM System Setup

Our ASIC was designed to operate in the 4×4 MIMO-OFDM testbed described in detail in [6]. Specifics of this testbed relevant to the ASIC design described in this paper are as follows: With an intermediate frequency (IF) of 20 MHz the sampling rate of the A/D and D/A converters is 80 Msps resulting in a baseband sampling rate of 20 Msps. The system clock frequency is 80 MHz. The same local oscillator is used for all antennas both at the transmitter and the receiver, respectively. Each receive RF chain contains a gain control element operated by the ASIC as explained in Section 3.1.

Table 1: IEEE 802.11a based modulation parameters.

Parameter	Value
FFT-length	$N_C = 64$ tones
Cyclic prefix	16 samples
Bandwidth	20 MHz
Symbol duration	4 μs
Modulation	BPSK, QPSK, 16-QAM

2.1 System Overview

The specifications of the MIMO-OFDM system under consideration are derived from the IEEE 802.11a WLAN

standard [4]; the corresponding high-level block diagram is shown in Figure 1.

In the transmitter, the high-rate data stream is first split into four parallel lower rate streams, which are OFDM-modulated (according to the IEEE 802.11a physical layer parameters summarized in Table 1) and sent through the MIMO channel. The received signals, consisting of a superposition of all transmitted signals, are then OFDM-demodulated, spatially separated and demultiplexed into a single high-rate stream. Our design does not include forward error correction coding.

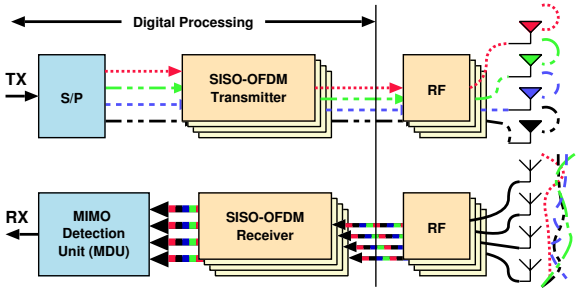

Figure 1: High-level block diagram of a MIMO-OFDM transceiver (top: transmitter, bottom: receiver).

2.2 Frame Structure

The frame structure proposed in the IEEE 802.11a standard has been adapted to the MIMO case as illustrated in Figure 2. The main difference to the single-antenna case lies in the short preamble sequence and the part of the frame containing the training symbols. The four different short preambles $\mathrm{SP_t}$ $(t = 1, ..., 4)$ are derived from the original IEEE 802.11a short preamble $\mathrm{SP_1}$ by tone-wise multiplication of the non zero entries of $\mathrm{SP_1}$ by different Hadamard codes; this avoids unintended beamforming, while still enabling the use of well-known SISO frequency offset estimation algorithms [7].

Compared to SISO systems, more training is needed to estimate the MIMO channel, which is due to the higher number of channel parameters in the MIMO case. To this end, each antenna transmits four OFDM training symbols $\mathrm{T_{tn}}$ $(t, n = 1, ..., 4)$ instead of the long preamble as specified in the IEEE 802.11a standard. The training symbols are orthogonal across antennas which is achieved by having only one antenna transmit on any given tone. K OFDM data symbols per antenna denoted as $\mathrm{D_{tk}}$ conclude the frame; the individual antennas transmit spatially independent data streams concurrently on all tones. Thus, the system operates in spatial multiplexing mode [2].

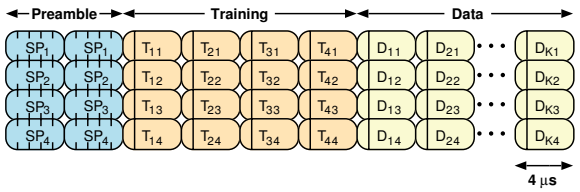

Figure 2: MIMO-OFDM frame structure. Each block corresponds to one OFDM symbol.

3. High-Level VLSI Architecture

Our ASIC is partitioned into three major blocks as shown in Figure 3. The block denoted as *multi-antenna OFDM processing* is responsible for OFDM de-/modulation and for frequency offset correction and frame start detection. The *MIMO detection unit* (MDU) is in charge of performing spatial separation of the individual data streams. Finally, a *FIFO buffer* is required to bridge the latency period incurred by the MDU. The system is externally configurable through an AMBA peripheral bus (APB).

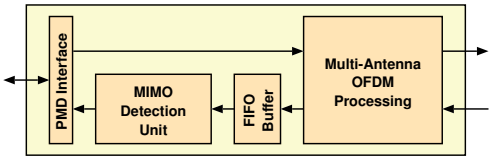

Figure 3: Block diagram of MIMO-OFDM transceiver.

3.1 Multi-Antenna OFDM Processing

We shall next describe the individual elements of the multi-antenna OFDM processing block depicted in Figure 4.

OFDM modulation and demodulation: The bit stream to be transmitted is mapped to QAM symbols followed by a 64-point IFFT, parallel-to-serial conversion and extension of the resulting time-domain sequence by a cyclic prefix of length 16. Since IEEE 802.11a is a time division duplex (TDD) system, the same hardware can be reused to perform the FFT. Moreover, one I/FFT hardware block is shared by the four transmit (receive) antennas. At the system clock frequency of 80 MHz, a single-butterfly radix-4 I/FFT was found to provide sufficient performance.

Digital up/down conversion: In order to reduce the number of required off-chip data converters and the associated large pin-count, I/Q de-/modulation is performed in the digital domain (using an IF of 20 MHz). This method also eliminates the problem of I/Q imbalance. However, the digital up-conversion (DUC) and the digital down-conversion (DDC) for the four antennas require a significant amount of registers and multipliers.

Automatic gain control (AGC): The considerable peak-to-average power ratio of OFDM signals renders AGC very important. We applied AGC to each antenna separately and used the following two-stage algorithm: The first stage generates a control signal for gain control in the analog domain. The second stage operates in the digital domain, at the input of the DDC. The AGC adjusts the signal level within 3.2 μs after the frame start.

Frequency offset estimation (FOE) and compensation: FOE is based on the Schmidl-Cox algorithm [7] with the corresponding autocorrelation function obtained by estimating a weighted (across the four antennas) correlation function; the weights are chosen to undo the effect of the second stage (digital part) of the AGC. The FOE block employs six real-valued multipliers. The frequency offset is compensated using one complex-valued multiplier in the frequency offset compensator (FOC) block.

Frame start detection (FSD): The start of a frame is detected by having the AGC detect a substantial power increase on at least three of the four receive antennas. The frame start detection process is assisted by the FOE block providing a metric indicating periodicity in the incoming signal which is a characteristic signature of the preamble of a frame.

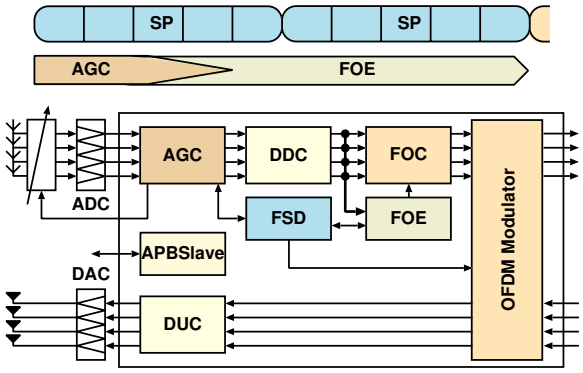

Figure 4: Different phases of frame acquisition (top) and block diagram of the multi-antenna OFDM processing unit (bottom).

3.2 MIMO Detection Unit

The use of OFDM converts the MIMO wideband channel into N_C parallel narrow-band MIMO channels so that detection of the spatially multiplexed data streams can be carried out on a tone-by-tone basis. The input-output relation for the i-th tone is given by

$$\mathbf{y}_i = \mathbf{H}_i \mathbf{s}_i + \mathbf{n}_i, \quad i = 1, ..., N_C \tag{1}$$

where $\mathbf{s}_i$ and $\mathbf{y}_i$ denote the transmitted and received vector respectively, $\mathbf{n}_i$ is thermal noise and $\mathbf{H}_i$ is the effective MIMO channel matrix corresponding to the i-th tone.
MIMO detection aims at estimating $\mathbf{s}_i$ from $\mathbf{y}_i$. To this end, a variety of algorithms can be employed [8, 2]. Optimum performance is achieved with maximum likelihood detection, implemented for example based on sphere decoding [9]. Unfortunately, even the fastest known ASIC implementation of the sphere decoder [10] does not achieve sufficient throughput for the MIMO-OFDM system under consideration. We therefore implemented an ordered successive interference cancellation scheme (OSIC) realizing a reasonable tradeoff between silicon complexity and performance. As outlined below, the ordering scheme employed in our case differs from the one used in the V-BLAST scheme [1]. In summary, the MIMO detection unit (MDU) carries out three major steps as illustrated in Figure 5 and described next.

Channel estimation: At the start of each frame, the channel matrices $\mathbf{H}_i$ need to be estimated based on the known training symbols. Due to the structure of the training symbols ensuring that only one antenna is active on each tone, the entries of $\mathbf{H}_i$ can be obtained from the received symbols in a straightforward way through hardware-inexpensive shift and sign-change operations. The result of the channel estimation process is a 4×4 matrix for each of the 64 tones. Using 20 bits to store a complex-valued matrix entry, 20 kbits of memory are required.

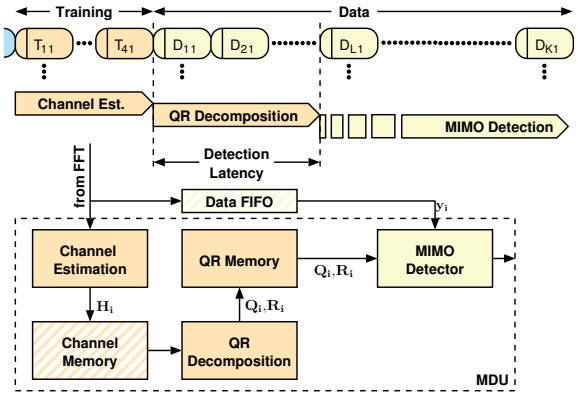

Figure 5: Timing diagram (top) and block diagram of MIMO detection (bottom).

QR-preprocessing: Once the matrices $\mathbf{H}_i$ have been estimated, the detection order is determined by ordering according to the column-norm of the $\mathbf{H}_i$ matrices. In contrast to the V-BLAST algorithm [1], we do not perform reordering in each step of the iterative detection process. This simplified ordering approach leads to hardware complexity savings due to increased regularity of the algorithm and a reduced number of operations. After rearrangement of the columns of the $\mathbf{H}_i$ matrices (according to the detection order), a per-tone QR-decomposition is performed to obtain $\mathbf{H}_i = \mathbf{Q}_i \mathbf{R}_i$ with $\mathbf{Q}_i$ unitary and $\mathbf{R}_i$ upper triangular. Since the training part of the frame is followed immediately by data and the detection process requires knowledge of all 64 matrix pairs $(\mathbf{Q}_i, \mathbf{R}_i)$, QR-preprocessing becomes a major bottleneck in terms of *detection latency*. Our ASIC design uses a moderately parallel architecture to perform QR-decomposition. This architecture is based on a single complex-valued CORDIC operating in vectoring mode and on a complex-valued Givens rotation block. The latter is implemented using three complex-valued multipliers, instead of CORDICs, which results in smaller silicon area and allows for a higher clock rate compared to a completely CORDIC-based implementation. A single QR-decomposition can be carried out in 65 clock cycles. The preprocessing latency caused by the per-tone QR-decomposition for all 64 tones adds up to a total of 52 μs. With an OFDM symbol duration of 4 μs, the *Data FIFO buffer* needs to be able to accommodate at least 13 OFDM symbols to bridge the QR-preprocessing latency. The corresponding 66 kbits of memory constitute a significant portion of the overall chip area (clearly visible in the top-left and bottom-left corners of the layout shown in Figure 6).

MIMO detection: MIMO detection starts upon completion of preprocessing and involves a matrix-vector multiplication [1] $\hat{\mathbf{y}}_i = \mathbf{Q}_i^H \mathbf{y}_i$ and back-substitution (BS) with slicing. Only five clock cycles are available per vector-symbol. In order to meet this demanding target, eight complex-valued multipliers are employed. Due to stringent dynamic range requirements in the BS process, the required precision of the variables involved imposes significant hardware complexity.

[1] $\mathbf{Q}^H$ denotes the Hermitian transpose of the matrix $\mathbf{Q}$.

4. Implementation Results

The layout of the MIMO-OFDM baseband signal processing ASIC described in this paper is shown in Figure 6. The area requirements of the different components described in Sections 3.1 and 3.2 along with the area requirements in a corresponding SISO system are summarized in Table 2. Most of the SISO components have to be replicated in the MIMO case which results in a fourfold chip area increase. The area occupied by the I/FFT processor increases only by 50% (compared to the SISO case) which is due to the fact that only one FFT block is used in the MIMO case with the same butterfly architecture as in the SISO case. The 50% area increase is therefore due to an increase in memory requirements in the MIMO case.

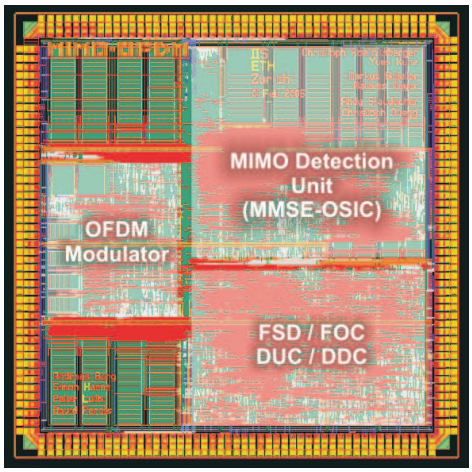

Figure 6: Layout of the MIMO-OFDM baseband signal processing ASIC manufactured in $0.25\ \mu m$ 1P/5M 2.5V CMOS technology.

The size of the data FIFO buffer and the latency incurred by QR-preprocessing can be reduced by reducing the algorithmic complexity of the QR-decomposition $\mathbf{H}_i = \mathbf{Q}_i\mathbf{R}_i$ $(i = 1, ..., 64)$. Corresponding algorithms exploiting the correlation between the $\mathbf{H}_i$ have recently been proposed in [11]. Another viable option for memory reduction is sharing of the same memory for the $\mathbf{H}_i$ and the $\mathbf{Q}_i$ matrices, which allows to save about half of the QR-memory. (These considerations also hold for other types of MIMO detectors like MMSE.)

Table 2: Chip area of baseband signal processing components in a $0.25\ \mu m$ CMOS technology.

Component	Area	
	SISO	4×4 MIMO
DDC, DUC	$0.5\ \mathrm{mm}^2$	$1.9\ \mathrm{mm}^2$
AGC	$0.1\ \mathrm{mm}^2$	$0.4\ \mathrm{mm}^2$
FOE, FOC, FSD	$0.3\ \mathrm{mm}^2$	$1.3\ \mathrm{mm}^2$
Modulator, I/FFT	$0.9\ \mathrm{mm}^2$	$1.4\ \mathrm{mm}^2$
Frame buffers	-	$3.3\ \mathrm{mm}^2$
Ch. est. & Ch. mem.	$<0.1\ \mathrm{mm}^2$	$1.12\ \mathrm{mm}^2$
QR-decomposition	-	$1.29\ \mathrm{mm}^2$
QR-memory	-	$1.23\ \mathrm{mm}^2$
MIMO detector	-	$0.9\ \mathrm{mm}^2$
Total	$1.9\ \mathrm{mm}^2$	$12.8\ \mathrm{mm}^2$

5. Conclusions

A 4×4 MIMO-OFDM WLAN baseband signal processing ASIC based on the IEEE 802.11a specifications has been presented. We observed that going from SISO to 4×4 MIMO the chip area increases by a factor of 6.5. Furthermore, the chip area occupied by the multi-antenna OFDM processing part is almost on par with the chip area corresponding to the MIMO detection unit. The main bottleneck was found to be the latency incurred by preprocessing the channel matrices for MIMO detection.

Acknowledgments

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